

## [ CLAIMS

We claim:

1           1.       A system for dynamically and automatically selecting a clock frequency  
2       for a resource accessed by zero or more controllers, wherein the clock frequency for the  
3       resource at least in part determines the bandwidth supported by the resource, the system  
4       comprising:

5               circuitry for generating a plurality of clocks of different frequencies;

6               circuitry for estimating the total bandwidth utilized by the zero or more  
7               controllers accessing the resource;

8               circuitry for dynamically and automatically selecting one of the plurality of  
9               clocks for the resource responsive to the estimated total bandwidth  
10              utilization; and

11              circuitry for providing the selected clock to the resource.

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2           2.       The system of claim 1, wherein the resource is a memory controller for  
3       controlling access to a memory using a memory clock and a clock enable signal and the  
4       system further comprises:

5               circuitry for disabling the clock enable signal if the estimated total bandwidth  
6               utilization for the controllers accessing the memory controller is zero;  
7               and

8               circuitry for disabling the memory clock responsive to the disabling of the  
9               clock enable signal.

1           3.       The system of claim 1, wherein the circuitry for estimating the total  
2       bandwidth utilized by the zero or more controllers accessing the resource comprises:  
3               a plurality of programmable registers, wherein each programmable register is  
4               associated with at least one controller capable of accessing the  
5               resource and each programmable register is adapted to hold a value

describing the bandwidth utilized by the at least one associated controller; and  
 adding circuitry in communication with the plurality of programmable registers for adding the values held in registers associated with controllers accessing the resource.

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4. The system of claim 1, wherein the circuitry for dynamically and automatically selecting one of the plurality of clocks for the resource responsive to the estimated total bandwidth utilization comprises:  
 a multiplexer having a plurality of inputs for receiving the plurality of clocks generated by the circuitry for generating a plurality of clocks and a selection input for receiving a selection value determined in response to the estimated total bandwidth utilized by the zero or more controllers accessing the resource.

5. The system of claim 4, further comprising:  
 a frequency table in communication with the selection input to the multiplexer and the circuitry for estimating the total bandwidth utilized by the zero or more controllers accessing the resource for outputting the selection value responsive to the estimated total bandwidth utilized by the zero or more controllers accessing the resource.

6. A portable electronic device comprising:  
 a plurality of resources for processing data, wherein the rate that a resource processes data is at least partially determined by a frequency of a clock received by the resource;  
 a clock generator for generating a plurality of clocks having different frequencies;  
 a plurality of controllers for accessing the resources, wherein each controller is adapted to access a resource at a given bandwidth; and

9 a clock controller in communication with the plurality of controllers and  
10 receiving the plurality of clocks, the clock controller adapted to  
11 dynamically and automatically select a clock of the plurality of clocks  
12 for a resource responsive to the bandwidth utilized by the controllers  
13 accessing the resource.

1           7.       The portable electronic device of claim 6, wherein the clock controller  
2 further comprises:  
3           a plurality of bandwidth registers, each bandwidth register associated with a  
4           particular controller in the portable electronic device and adapted to  
5           hold a value representative of the bandwidth utilized by the associated  
6           controller.

1           8.       The portable electronic device of claim 7, wherein the clock controller  
2 further comprises:  
3           an adder for summing the contents of the bandwidth registers associated with  
4           the controllers in the portable electronic device accessing the resource.

ba3 9. The portable electronic device of claim 8, further comprising:  
a frequency table having entries describing clock frequencies for a resource in  
the portable electronic device, wherein the sum produced by the adder  
is an index to an entry in the frequency table.

1           10.     The portable electronic device of claim 8, wherein the clock controller  
2 further comprises:  
3           a multiplexer for receiving the plurality of clocks generated by the clock  
4           generator and outputting a clock selected responsive to the sum  
5           produced by the adder.

1            11.    The portable electronic device of claim 10, further comprising circuitry for  
2    applying the selected clock to the resource.

12. The portable electronic device of claim 8, wherein the plurality of resources comprise:

- a bus for transferring information among ones of the plurality of controllers in communication with the bus;
- a memory controller in communication with the bus for controlling access to at least one external memory device by ones of the plurality of controllers; and
- a central processing unit controller in communication with the bus for controlling accesses to a central processing unit by ones of the plurality of controllers.

<sup>12</sup>  
~~13.~~ The portable electronic device of claim <sup>11</sup>~~12~~, wherein the memory controller communicates with the external memory device using a clock and a clock enable signal and the portable electronic device further comprises:

- circuitry for disabling the clock enable signal when the bandwidth utilized by the controllers accessing the memory is zero; and
- circuitry for terminating the memory clock when the clock enable signal is disabled.

14. A method of selecting one of a plurality of clocks having different frequencies for a resource, wherein the clock frequency determines at least in part the bandwidth that the resource can process, comprising the steps of:

- determining whether zero or more controllers are accessing the resource;
- estimating bandwidth utilized by the zero or more controllers accessing the resource;
- dynamically and automatically selecting one of the plurality of clocks responsive to the estimated bandwidth utilized by the zero or more controllers accessing the resource; and
- applying the selected clock to the resource.

1           15.    The method of claim 14, wherein the step of estimating bandwidth utilized  
2 by the zero or more controllers accessing the resource comprises the steps of:  
3            assigning a value to each controller representative of the bandwidth utilized by  
4            that controller; and  
5            summing the values assigned to the controllers that are accessing the resource.

1           16.    The method of claim 15, wherein the step of dynamically and  
2 automatically selecting one of the plurality of clocks responsive to the estimated  
3 bandwidth utilized by the zero or more controllers accessing the resource comprises the  
4 step of:  
5            selecting one of the plurality of clocks with the sum.

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1           17.    The method of claim 14, wherein the resource is a memory controller and  
2 the determining step determines that zero controllers are accessing the memory controller,  
3 further comprising the steps of:  
4            disabling a clock enable signal from the memory controller; and  
5            disabling a clock to the memory controller.

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1           18.    An application-specific integrated circuit for processing data, the circuit  
2 comprising:  
3            a plurality of programmable registers for holding values, wherein each register  
4            is adapted to hold a value describing data processing rate of an  
5            associated device;  
6            an adder in communication with the plurality of programmable registers for  
7            summing the values in ones of the plurality of registers associated with  
8            devices accessing a resource, wherein the sum describes the total data  
9            processing rate of the devices accessing the resource; and  
10           selection circuitry in communication with the adder for selecting one of a  
11           plurality of clock frequencies for the resource responsive to the sum  
12           produced by the adder.

1       <sup>16</sup>  
19.       The application-specific integrated circuit of claim <sup>15</sup>18, further comprising:  
2       a frequency table in communication with the adder and the selection circuitry  
3       for converting the sum produced by the adder into a selection value for  
4       use by the selection circuitry for selecting one of the plurality of clock  
5       frequencies.

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